

1. $V_{CTL(H)}=1.8V / f=0.5 - 3.0GHz$ APPLICATION

1-1 SUMMARY

This is $V_{CTL(H)}=1.8V / f=0.5 - 3.0GHz$ application note of NJG1801K75.

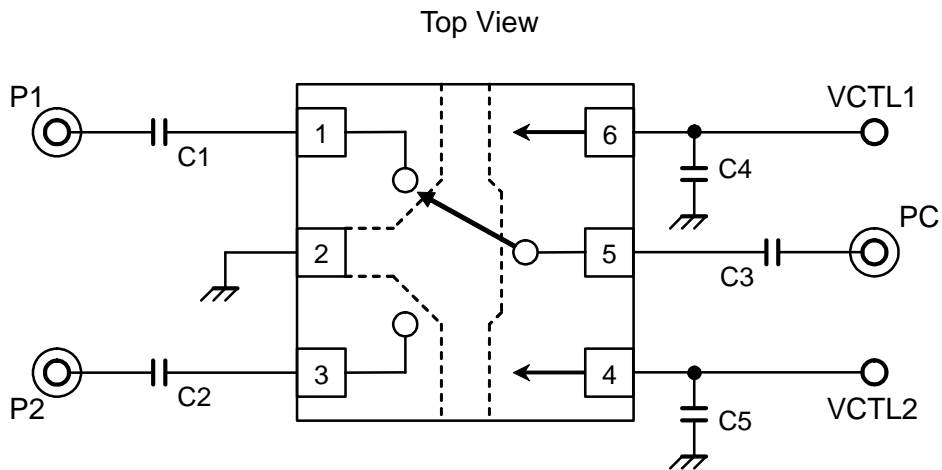
This application note shows the typical electrical characteristics and application circuit.

1-2 MEASURED DATA

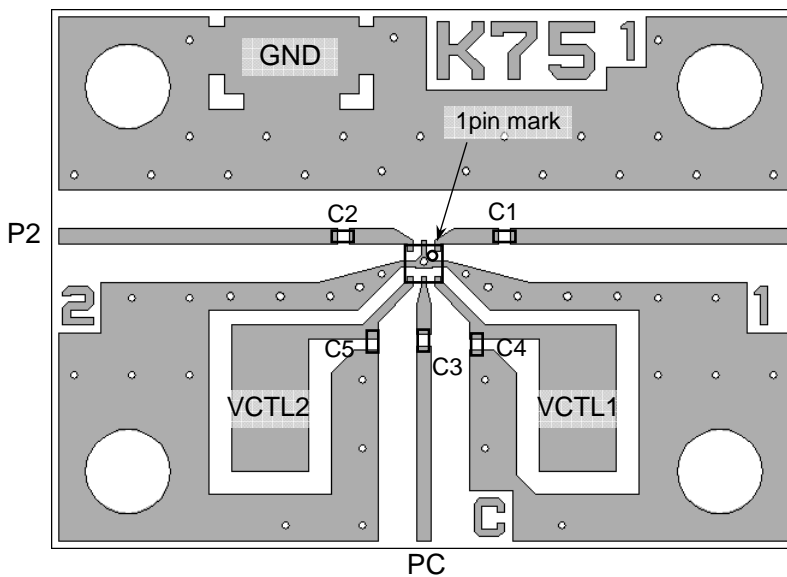
General conditions: $V_{CTL(L)}=0V$, $V_{CTL(H)}=1.8V$, $T_a=+25^{\circ}C$, $Z_S=Z_I=50\Omega$

PARAMETERS	SYMBOL	CONDITIONS	DATA	UNITS
Control Current	I_{CTL}	$V_{CTL(H)}=1.8V$, No RF input	2.7	μA
Insertion loss1	LOSS1	$f=0.5GHz$	0.30	dB
Insertion loss2	LOSS2	$f=1.0GHz$	0.31	dB
Insertion loss3	LOSS3	$f=2.0GHz$	0.33	dB
Insertion loss4	LOSS4	$f=2.7GHz$	0.34	dB
Isolation1	ISL1	$f=0.5GHz$	34.8	dB
Isolation2	ISL2	$f=1.0GHz$	30.0	dB
Isolation3	ISL3	$f=2.0GHz$	27.5	dB
Isolation4	ISL4	$f=2.7GHz$	27.6	dB
Return loss1	RL1	$f=0.5GHz$	18.9	dB
Return loss2	RL2	$f=1.0GHz$	23.8	dB
Return loss3	RL3	$f=2.0GHz$	28.3	dB
Return loss4	RL4	$f=2.7GHz$	29.9	dB
Input power at 1dB compression point1	P_{-1dB1}	$f=1.0GHz$	24.8	dBm
Input power at 1dB compression point2	P_{-1dB2}	$f=2.0GHz$	24.0	dBm
Switching time	T_{SW}	50% V_{CTL} to 10%/90% RF	272	ns

1-3 APPLICATION CIRCUIT



1-4 PCB DESIGN



PCB: FR-4, t=0.2mm
 Capacitor Size: 0603 (0.6 x 0.3 mm)
 Strip Line Width: 0.4mm
 PCB Size: 19.4 x 14.0mm
 Through Hole Diameter: 0.2mm

■ Loss of PCB, capacitor and connectors

Frequency (GHz)	Loss (dB)
0.5	0.15
1.0	0.17
2.0	0.26
2.7	0.34

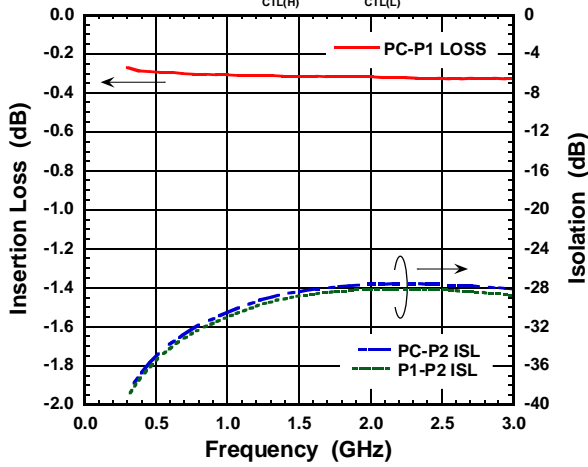
PARTS LIST

Parts ID	Constants	Comment
C1 to C3	56pF	Murata MFG (GRM03 series)
C4 to C5	10pF	

1-5-1 Characteristics

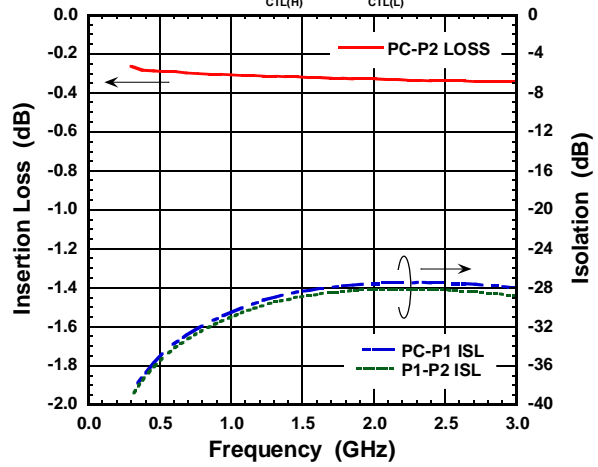
Loss, ISL vs Frequency

(PC-P1 ON, $V_{CTL(H)}=1.8V$, $V_{CTL(L)}=0V$)



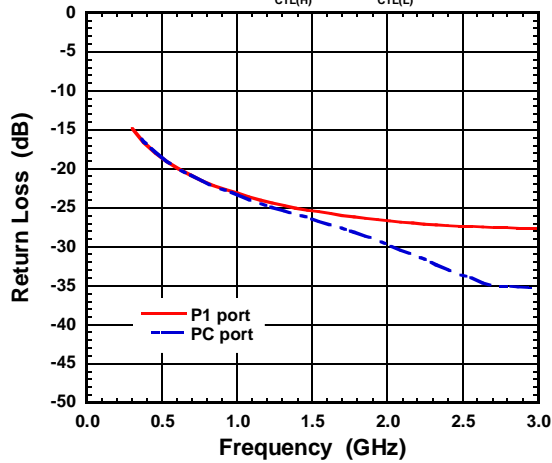
Loss, ISL vs Frequency

(PC-P2 ON, $V_{CTL(H)}=1.8V$, $V_{CTL(L)}=0V$)



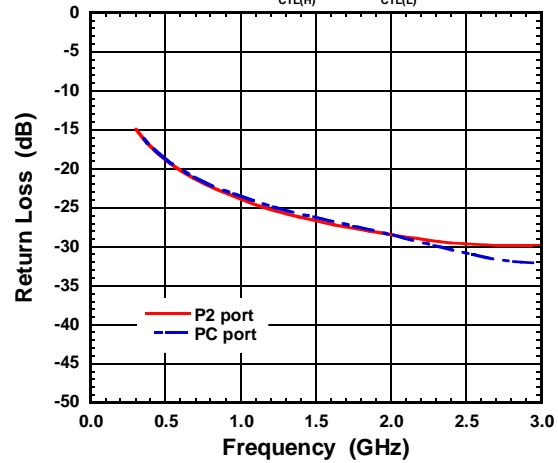
Return Loss vs Frequency

(PC-P1 ON, $V_{CTL(H)}=1.8V$, $V_{CTL(L)}=0V$)



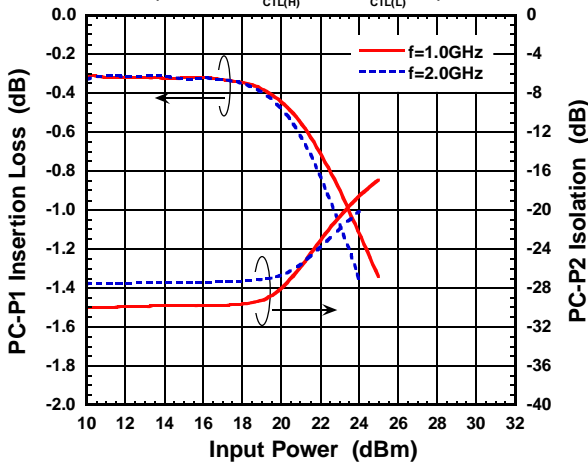
Return Loss vs Frequency

(PC-P2 ON, $V_{CTL(H)}=1.8V$, $V_{CTL(L)}=0V$)



Loss, ISL vs Input Power

(PC-P1 ON, $V_{CTL(H)}=1.8V$, $V_{CTL(L)}=0V$)



Loss, ISL vs Input Power

(PC-P2 ON, $V_{CTL(H)}=1.8V$, $V_{CTL(L)}=0V$)

