



0.35 um BCD
for
High Voltage Products with Logic

Process Code: UD50

July 30, 2010

New Japan Radio Co., Ltd.

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Process Features

Substrate 8inch P-sub.with N-epi.

Gate Length 0.35um (3.3V CMOS)

Gate Oxide 70 / 120

Interconnect 2Poly 3Metal
(5 Metal is ready, if required)

Metal Thickness

Top Metal 0.8um or 3.0um

Others 0.5um

Silicide Ti Salicide

Isolation LOCOS

Devices

LDMOS Nch 40V / 50V

Pch 40V / 50V

HVMOS Pch 50V

LV CMOS 3.3V / 5.0V

Bipolar NPN 15V

Lateral PNP 15V

Zener Diode $V_z = 5.2V$

Capacitor PIP 1.6 fF/um² for 5V

PIP 0.85 fF/um² for 15V

MOS 2.6 fF/um² for 5V

Resistor

Poly Si for HV and LV 2k / 640 / 51 ohm/sq.

Implant for LV 1,700 / 200 / 75 ohm/sq.

Poly Fuse for Laser zap

OTP (supplied by eMemory)

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